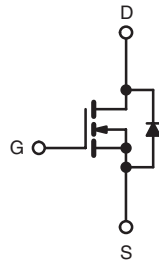
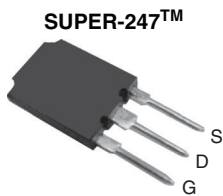


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	600	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	0.110
Q_g (Max.) (nC)	330	
Q_{gs} (nC)	84	
Q_{gd} (nC)	150	
Configuration	Single	



N-Channel MOSFET

FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Enhanced Body Diode dV/dt Capability
- Lead (Pb)-free Available


RoHS*
COMPLIANT

APPLICATIONS

- Hard Switching Primary or PFC Switch
- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Motor Drive

ORDERING INFORMATION

Package	Super-247™
Lead (Pb)-free	IRFPS40N60KPbF
	SiHFPS40N60K-E3
SnPb	IRFPS40N60K
	SiHFPS40N60K

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted


PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current ^a	I_{DM}	160	
Linear Derating Factor		4.5	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	600	mJ
Repetitive Avalanche Current ^a	I_{AR}	40	A
Repetitive Avalanche Energy ^a	E_{AR}	57	mJ
Maximum Power Dissipation	$T_C = 25$ °C	P_D	W
Peak Diode Recovery dV/dt^c		dV/dt	5.5
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25$ °C, $L = 0.84$ mH, $R_G = 25$ Ω , $I_{AS} = 38$ A, $dV/dt = 5.5$ V/ns (see fig. 12).
- $I_{SD} \leq 38$ A, $dI/dt \leq 150$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.22	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	600	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$	-	0.63	-	V/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.0	-	5.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	50	μA	
		$V_{DS} = 480\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 24\text{ A}^b$	-	0.110	0.130	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 24\text{ A}^b$	21	-	-	S	
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5	-	7970	-	pF	
Output Capacitance	C_{oss}		-	750	-		
Reverse Transfer Capacitance	C_{rss}		-	75	-		
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}$, $f = 1.0\text{ MHz}$	-	9440	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 480\text{ V}$, $f = 1.0\text{ MHz}$	-	200	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$V_{DS} = 0\text{ V to } 480\text{ V}^c$	-	260	-	
Gate-Source Charge	Q_{gs}		$I_D = 38\text{ A}$, $V_{DS} = 480\text{ V}$, see fig. 6 and 13 ^b	-	-	330	nC
Gate-Drain Charge	Q_{gd}			-	-	84	
Turn-On Delay Time	$t_{d(on)}$			-	47	-	
Rise Time	t_r	$V_{DD} = 300\text{ V}$, $I_D = 38\text{ A}$, $R_G = 4.3\text{ }\Omega$, see fig. 10 ^b	-	110	-	ns	
Turn-Off Delay Time	$t_{d(off)}$		-	97	-		
Fall Time	t_f		-	60	-		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	40	A	
Pulsed Diode Forward Current ^a	I_{SM}		-	-	160		
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 38\text{ A}$, $V_{GS} = 0\text{ V}^b$	-	-	1.5	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$	-	630	950	ns	
		$T_J = 125\text{ }^\circ\text{C}$	-	730	1090		
Body Diode Reverse Recovery Charge	Q_{rr}	$T_J = 25\text{ }^\circ\text{C}$	$I_F = 38\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	14	20	μC
		$T_J = 125\text{ }^\circ\text{C}$		-	17	25	
Body Diode Recovery Current	I_{RRM}	$T_J = 25\text{ }^\circ\text{C}$	-	39	58	A	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS} .

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

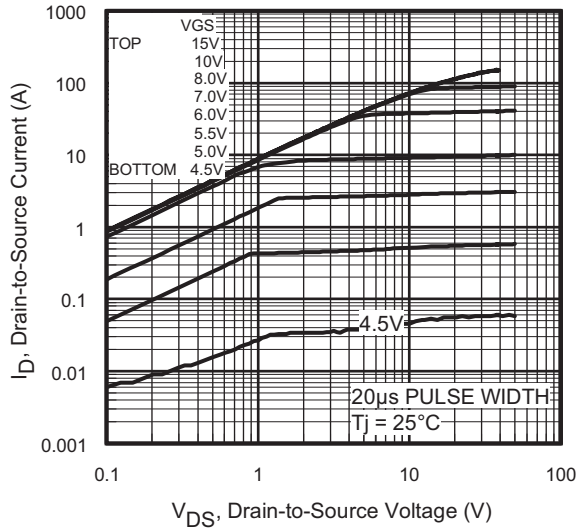


Fig. 1 - Typical Output Characteristics

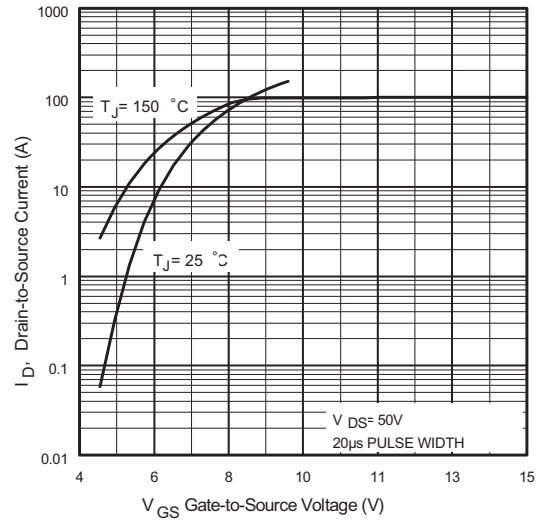


Fig. 3 - Typical Transfer Characteristics

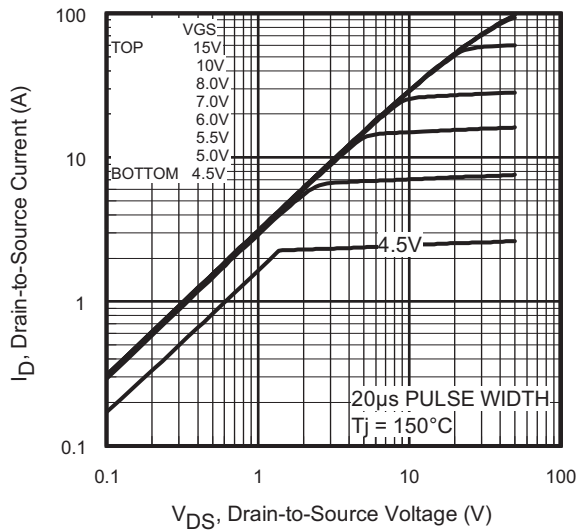


Fig. 2 - Typical Output Characteristics

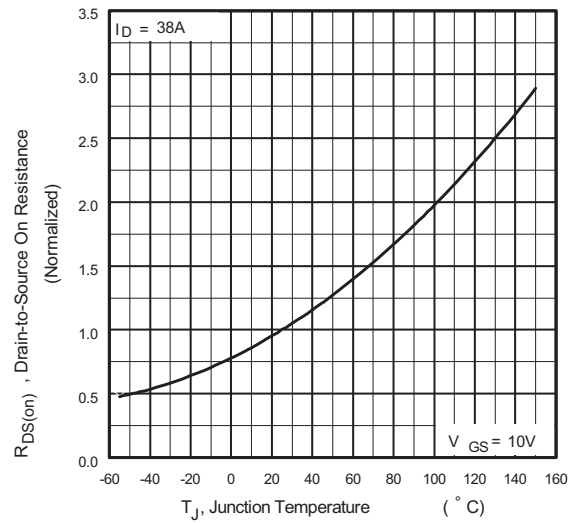


Fig. 4 - Normalized On-Resistance vs. Temperature

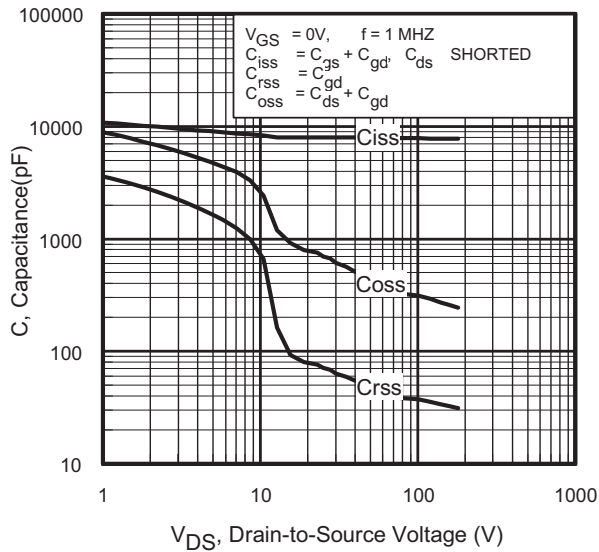


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

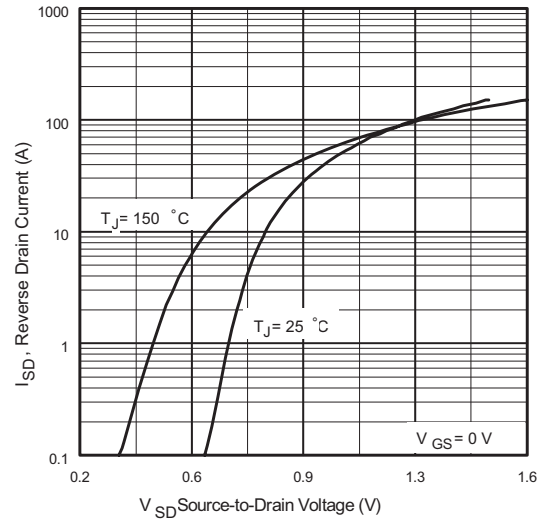


Fig. 7 - Typical Source-Drain Diode Forward Voltage

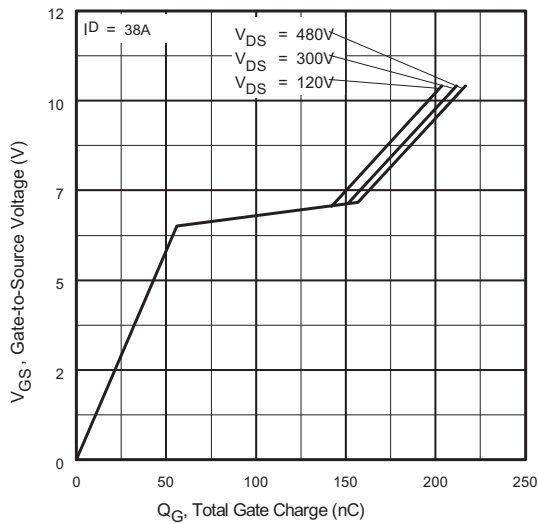


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

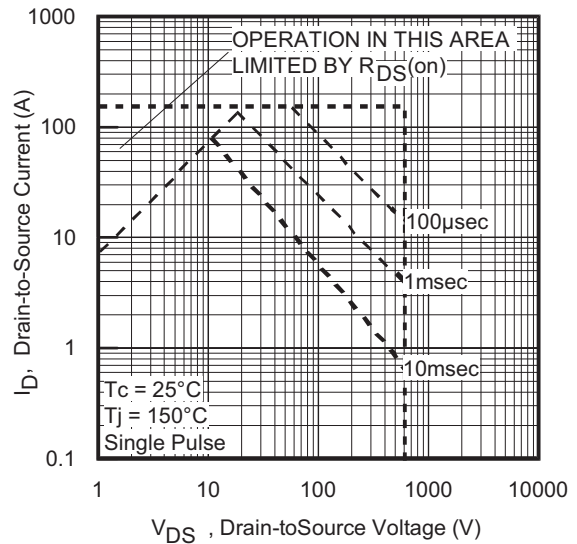


Fig. 8 - Maximum Safe Operating Area

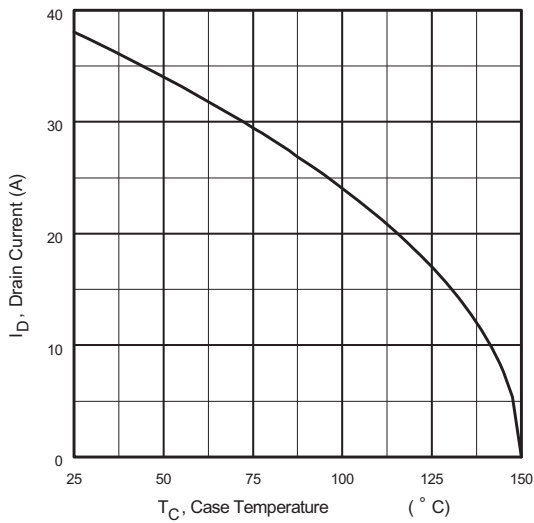


Fig. 9 - Maximum Drain Current vs. Case Temperature

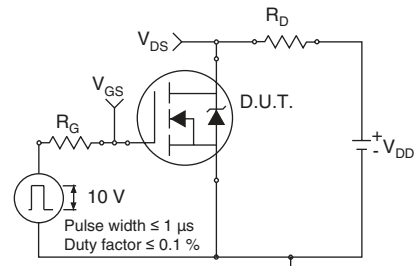


Fig. 10a - Switching Time Test Circuit

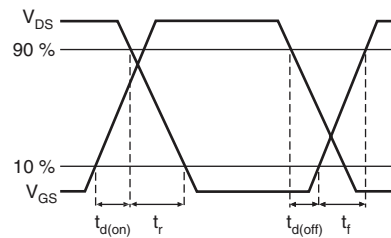


Fig. 10b - Switching Time Waveforms

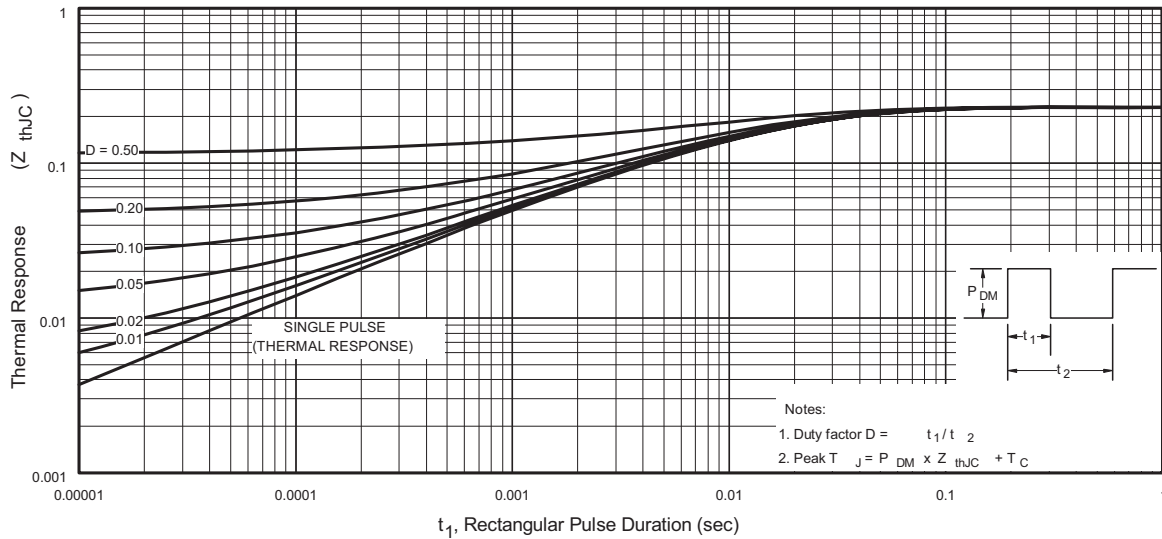


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

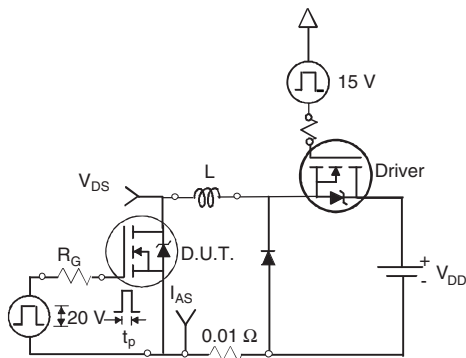


Fig. 12a - Unclamped Inductive Test Circuit

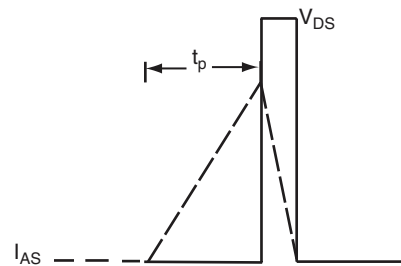


Fig. 12b - Unclamped Inductive Waveforms

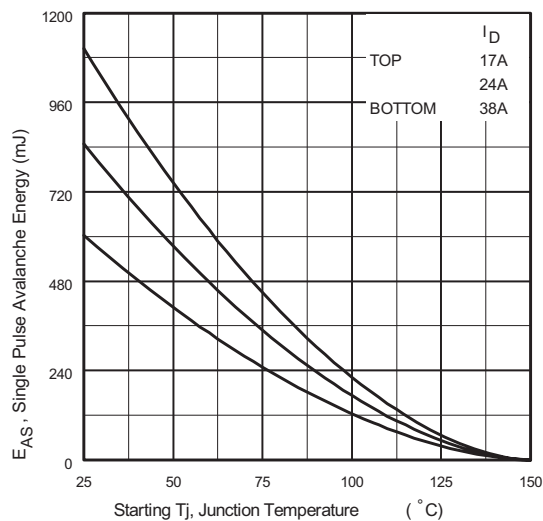


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

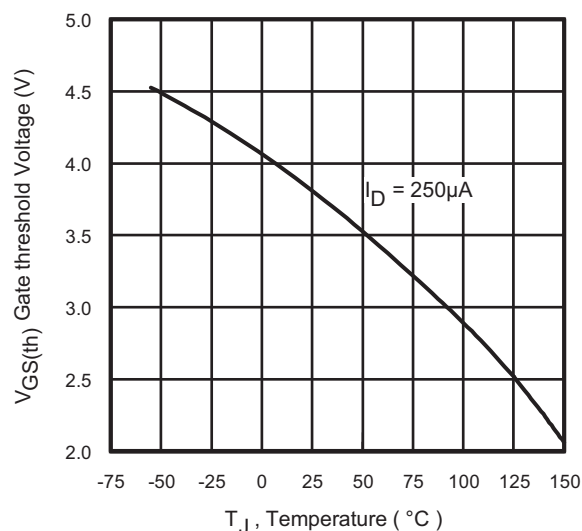


Fig. 12d - Threshold Voltage vs. Temperature

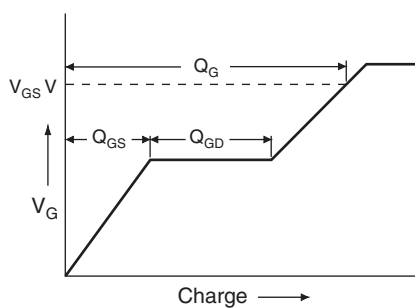


Fig. 13a - Basic Gate Charge Waveform

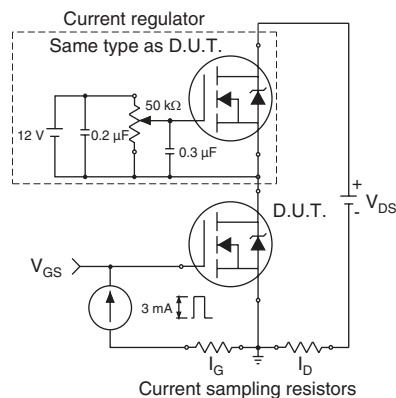


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

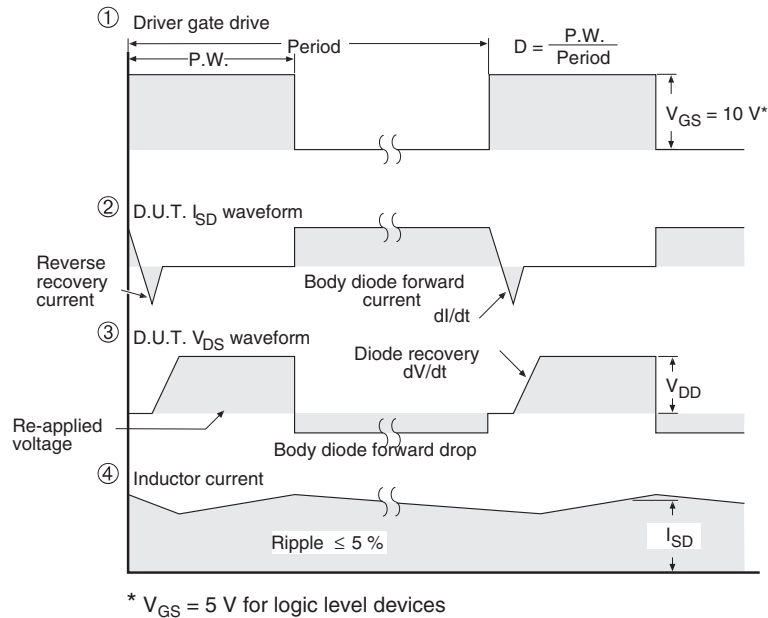
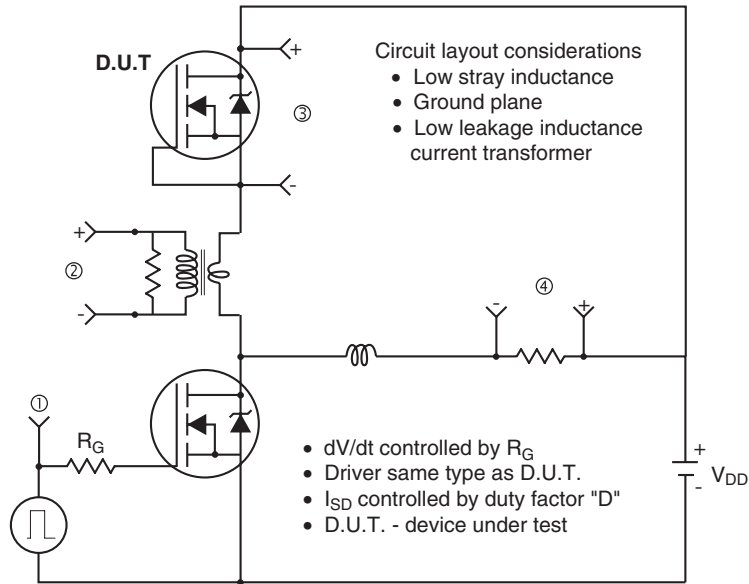


Fig. 14 - For N-Channel

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